Final Report on the Project for Development of New Protocol Hardware and Software for LSI-11 to Accommodate AUTODIN II ADCCP-HDLC, and X.25

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Appendix A

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XQCP.MM.V004
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XQ/CP

MAINTENANCE MANUAL

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MAINTENANCE MANUAL

CHAPTER 1 - INTRODUCTION

CHAPTER 1

1.0 INTRODUCTION

1.1 Maintenance Manual Contents- This manual contains information on the application, installation, operations, and maintenance of the XQ/CP. Included is information on physical characteristics, logic operations, programming, and interface specifications.

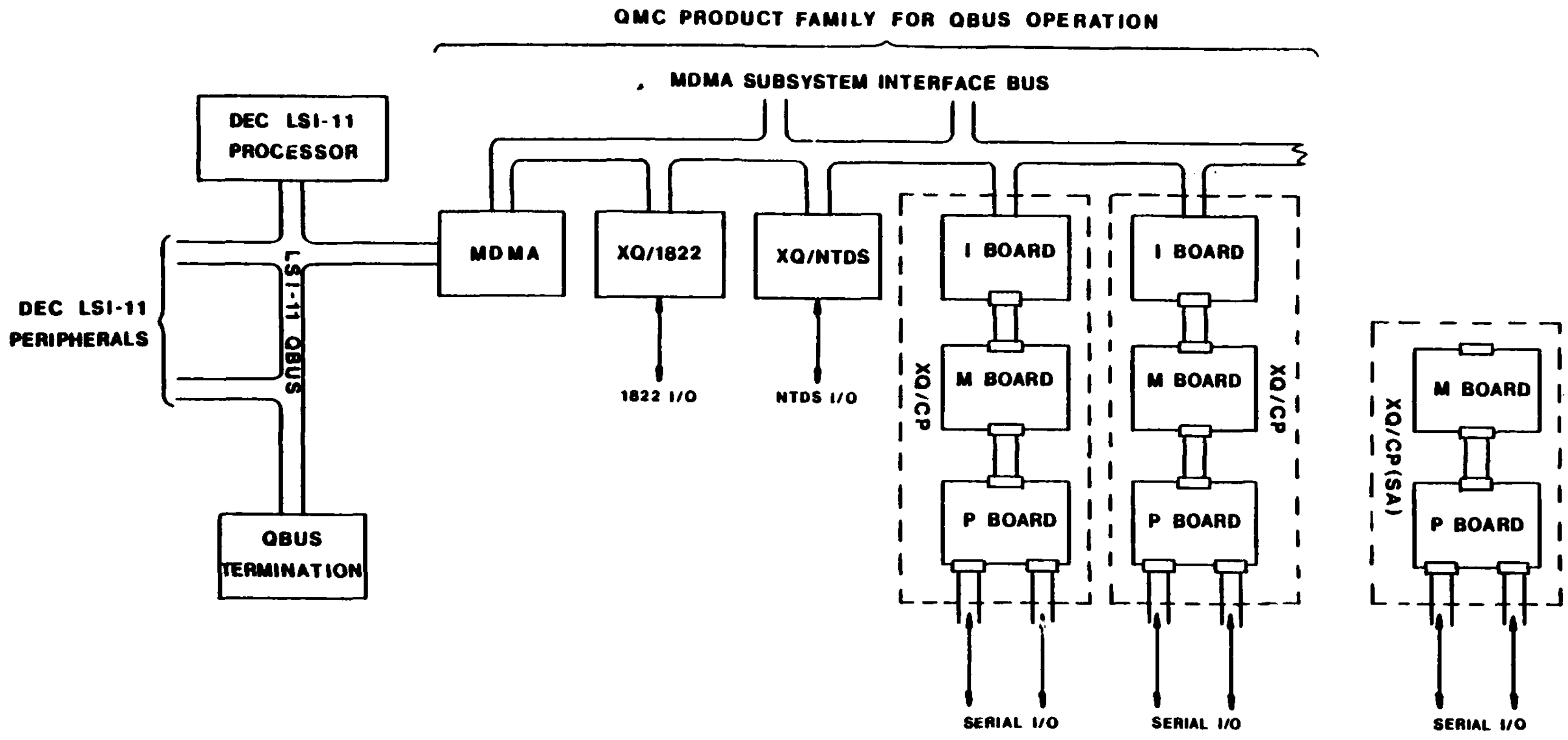
1.2 Description - The XQ/CP is a communication processor that can be programmed to deal with telecommunication protocols, the pre- and post-processing of information, and general applications that are suitable for microprocessor execution. The XQ/CP can be operated as a stand-alone unit or as an intelligent peripheral attachment to the DEC LSI-11 system, as shown in Figure 1-1.

1.3 XQ/CP Interconnection and Configuration - The XQ/CP comprises three circuit boards that are interconnected, as shown in Figure 1-1 and Figure 1-2. When tied into the DEC LSI-11 QBUS, the use of a Multichannel Direct Memory Access (MDMA) circuit board is required along with the XQ/CP Boards.

The I-Board provides the interface between the XQ/CP External Microprocessor Bus and the MDMA Subsystem Interface Bus (SIB). The MDMA is a communications controller that allows multiple attachments to operate in the DMA mode with the LSI-11. (KP)

1.4 XQ/CP Features - The XQ/CP provides two complete DMA channels to the LSI-11 QBUS via the MDMA and supports two full duplex serial I/O channels that operate under DMA control with the XQ/CP memory. Other features include an on-board baud rate generator, a counter timer, and the capability to jumper in an on-board clock source in order to support stand alone operation.

1.5 Physical Characteristics - The XQ/CP is packaged on three standard dual-height, extended length LSI-11 printed circuit boards. The three boards are the I-Board (Interface), M-Board (Memory), and P-Board (Processor). The I-Board connects to the MDMA Subsystem Interface Bus via a 40 conductor flat cable that may be part of a multi-hop arrangement for multiple device interconnection. The P-Board provides two serial I/O connections by means of similar cabling. The three boards connect via the External Microprocessor Bus. This bus is configured with two connectors on each board one input and one output (the P-Board has one connection). Expansion of the microprocessor facilities is possible via this bus. Figure 1-2 shows the connections of the three boards with the MDMA board which is also a dual-height board.



NOTE: XQ/CP shown interconnected with LSI-11 by way of the MDMA Controller and in the stand-alone configuration XQ/CP(SA).

Figure 1-1 XQ/CP Interconnection And Configuration With Other Units

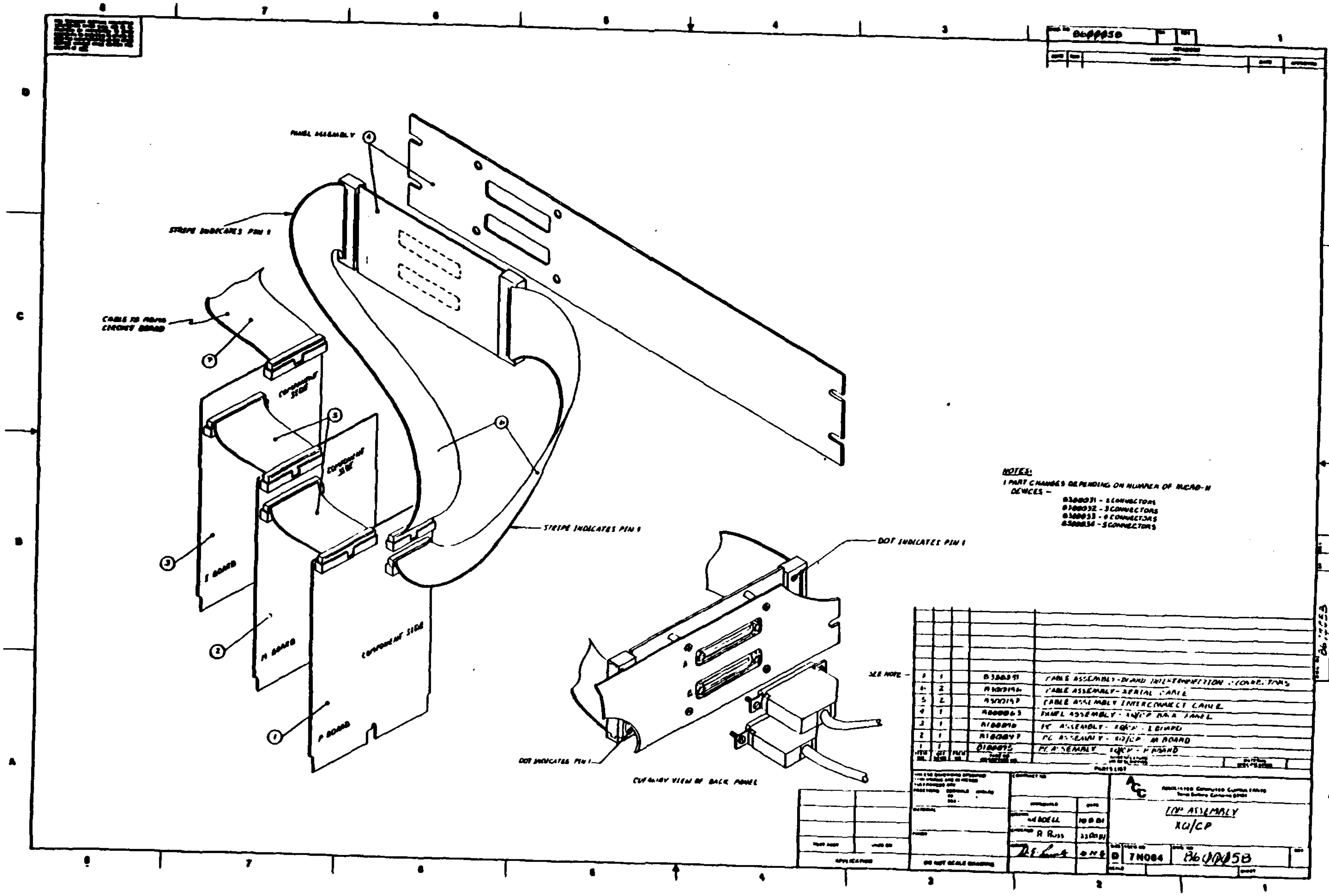


Figure 1-2 Top Assembly XQ/CP

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CHAPTER 2 - REFERENCES

CHAPTER 2

2.0 REFERENCES

2.1 Reference Documents

2.1 Reference Documents - Pertinent documents for programming, maintaining, and operating the XQ/CP are listed below:

1. Microcomputer Processors
   Digital Equipment Corporation

2. Schottky and Low-Power Schottky Data Book
   Advanced Micro Devices, Inc.

3. The TTL Data Book
   Texas Instruments, Inc.

4. Bipolar Microcomputer Components Data Book
   Texas Instruments, Inc.

5. Memory Data Book and Designers' Guide
   Mostek Corporation

6. Microcomputer Components Data Book
   Zilog, Inc.

7. Maintenance Manual: MDMA
   Associated Computer Consultants, MDMA.MM.V001

8. PDP-11 Macro-11 Language Reference Manual
   Digital Equipment Corporation

9. Reference Manual for the Microbench Z80
   Program Development Systems
   Virtual Systems, Inc.

10. Z80 CPU Technical Manual
    Zilog, Inc.

11. XQ/CP Software Support Monitor Manual
    Associated Computer Consultants, XQCP.SSMM.V001

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CHAPTER 3 - GENERAL DESCRIPTION

CHAPTER 3

3.0 GENERAL DESCRIPTION

3.1 Packaging - The XQ/CP is packaged on three LSI-11 QBUS compatable dual-height printed circuit boards. These boards plug directly into the QBUS backplane. The serial I/O line connectors are mounted on a standard 19 inch, rack mountable panel.

3.2 Alternate XQ/CP Board Arrangement - The three boards may be connected in the two ways that are shown in Figure 3-1 on the next page.

3.2.1 External Microprocessor Bus Interconnector - The External Microprocessor Bus has its source on the P-Board connector J1. Both the M-Board and the I-Board have an input connector (J2) and output connector (J1). These boards may be connected in either order shown. The connectors have been designed so that internal cables do not cross external cables (see Figure 1-2).

3.2.2 MDMA Subsystem Interface Bus Interconnection - The I-Board provides the connection to the MDMA board via J3. MDMA Subsystem Interface Bus continuation is taken from J3.

3.2.3 Serial I/O Connection - Serial I/O connection is provided by P-Board connectors J2 and J3. J2 is I/O Channel A and J3 is I/O Channel B. Serial connection supports RS-232, RS-449, or MIL-STD-188-114. The receptacles on the serial I/O connector are either 25-pin or 37-pin according to the application.

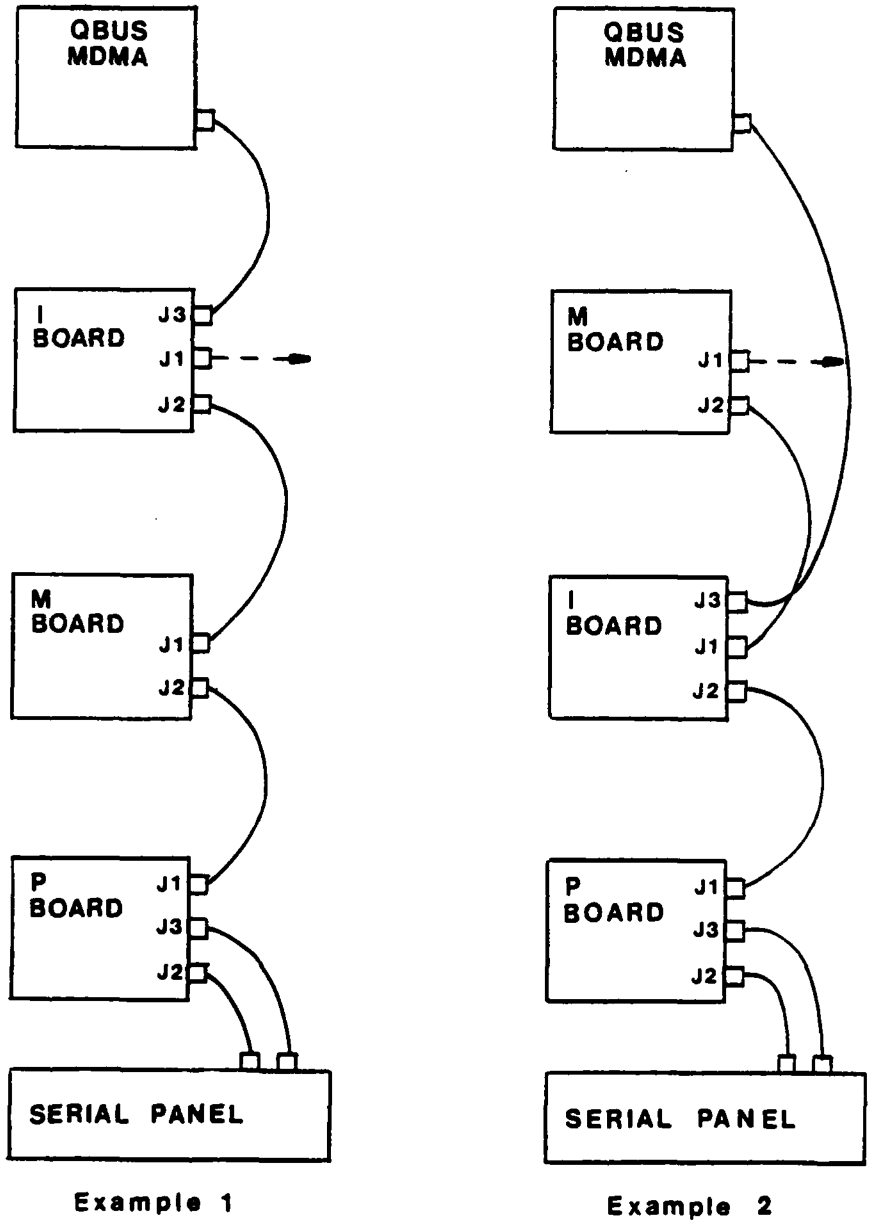

Figure 3-1 Interconnection Diagram

3.3 Functional Description - The XQ/CP is a microprocessor device that communicates via two full duplex serial ports and via the MDMA Subsystem Interface Bus (see Block Diagram 2700060 sheet 1, in Appendix A). The microprocessor is a Zilog Z80-CPU. Standard Zilog peripherals have been attached to the microprocessor bus to achieve the functional requirements of the XQ/CP. These include a Z80-CTC for counter-timer and interrupt functions, a DMA controlled Z80-SIO (Serial Input/Output) for high speed serial communications, and two additional Z80-DMA's for controlling data transfers in each direction on the MDMA Subsystem Interface Bus. Other attachments have been made to the microprocessor bus in order to support the functional requirements of the XQ/CP. These include RAM up to 32K X 8, ROM up to 32K X 8, a baud rate generator, and communications registers that provide data and control for Direct Memory Access (DMA) block transfers. The XQ/CP starts operation at memory location 0000 after a reset.

3.4 Processor Module - The P-Board contains the basic Z80 microprocessor components (refer to the P-Board Block Diagram, Drawing 2700060, sheet 2 in Appendix A). All Z80 components communicate on a common bus. This bus contains data, address, and control bits that operate according to rules specified by Zilog. A separate address decoder recognizes I/O port addresses and provides the enable signal for the Z80-CTC (Counter-Timer), Z80-DMA's, Z80-SIO, and an on-board baud rate generator.

3.4.1 The Z80-CTC - The Z80-CTC provides a four channel counter/timer. One channel is dedicated to providing a mechanism for off-board interrupts. The other three channels may be used by the programmer for general applications.

3.4.2 The Z80-SIO - The Z80-SIO provides two full duplex serial I/O channels. The serial line interface will meet the electrical specifications of one of the following standards: RS-232, RS-449, or MIL-STD-188-114. There is a Z80-DMA for each of the serial channels to support high speed applications. The serial channels can be microprogrammed to run under full DMA control or to be directly controlled by the CPU.

3.4.3 External Microprocessor Bus - The P-Board has drivers and receivers for the External Microprocessor Bus in order to provide a completely buffered external bus for the other boards of the system.

3.5 Memory Module - The M-Board contains all memory directly addressed by the XQ/CP's CPU. The External Microprocessor Bus is completely buffered and decodes according to a memory mapping ROM. This ROM determines the response addresses of RAM and ROM. Each of these areas of memory is expandable up to 32K X 8. The RAM is expandable in increments of 16K; the ROM is expandable in increments of 4K or 8K (refer to the M-Board Block Diagram, Drawing 2600060, sheet 3 in Appendix A).

3.6 Interface Module - The I-Board provides the data path between the External Microprocessor Bus and the MDMA Subsystem Interface Bus (see the I-Board Block Diagram, Drawing 2600060, sheet 4 in Appendix A).

3.6.1 DMA Paths For External Microprocessor Bus - From the point of view of the Z80-CPU, two independent DMA paths exist: one for reading data blocks and one for writing data blocks. Each path is fully controlled by a Z80-DMA, which contains the transfer count, memory address, status, and control. The Z80-DMA obtains complete control of the Z80 bus and accomplishes a block transfer without Z80-CPU intervention.

3.6.2 Data Path for MDMA Subsystem Interface Bus - Control of the Subsystem Interface Bus side of the data paths and manipulation of the Communication Register is done by the MDMA. The initial parameters are loaded into the Address and Count Registers by a program residing in the LSI-11.

3.6.3 Block Transfer Process - Data transfer is initiated by setting the appropriate bit in the Control Register. If the Z80-CPU has also completed the necessary initialization of its side of the DMA path, then the block transfer will take place. Note that each process provides only the parameters for its side of the data path and is not cognizant of any other process's parameters. Control information may be passed through the corresponding Control Registers. The conversion of 16-bit word length to 8-bit word length is accomplished by special hardware. The I-board also does MDMA Subsystem Interface Bus decoding and has switch settings to provide an Interrupt Vector and Identification Code.

3.7 Special Features - The XQ/CP has a number of features that allow for different configurations, component options, interface options, and expandability. A summary of these features is provided in subsequent paragraphs.

3.7.1 Stand Alone Mode - Although the XQ/CP is normally configured as a peripheral on the MDMA Subsystem Interface Bus, it may be used as a stand alone CPU. This is accomplished by jumpering in a clock generator on the P-Board (see Section 4-4). Additionally, a reset pulse must be provided so that program control begins from a known state.

3.7.2 Serial Interface Options - The serial interface may be specified to be one of the following standards: RS-232, RS-449, or MIL-STD-188-114. This is accomplished by component platforms on the P-Board. These are installed by the factory, but they may be changed in the field.

3.7.3 Memory Options - Memory options are available that determine the size, configuration, speed, and ROM type. The speed and ROM types are established by the factory based on availability of parts. The standard size and configuration options are 32K bytes of RAM and 32K bytes of ROM with the ROM occupying the lower half of the address space (see Figure 3-2). Other configurations are possible. For example, if a system is to be used in a development environment, a minimal amount of ROM might be desired as in Figure 3-3. Large fixed applications could be configured as in Figure 3-4. RAM is available as 16K X 8 or 32K X 8. ROM is available in 4K X 8 increments up to 32K X 8 or in 8K X 8 increments up to 64K X 8.

3.7.4 Switch Register and Display Register - A DIP switch may be used to enter data to the XQ/CP. It is available as an I/O port on the microprocessor bus. A set of LED's are also implemented as an I/O port to display a byte of information. These facilities may be used in diagnostic, or other special purpose software, to obtain manually entered data or to display status information.

3.7.5 External Microprocessor Bus - The XQ/CP provides a completely buffered set of bus signals that is output on J1 of any of the boards. This bus provides the XQ/CP with two appealing characteristics: modularity and expandability. The modularity that has been achieved in the packaging of the XQ/CP allows it to be either an MDMA Subsystem Interface Bus peripheral or a stand alone microprocessor (without the I-Board). If it is desired to interface the XQ/CP to a different device, the I-Board can be replaced by different interface hardware. Similiarly, a different memory board can be designed and different Z80 peripherals can be added to the Z80 bus.

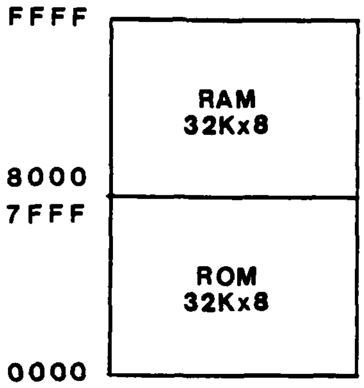

Figure 3-2 Standard Memory Configuration

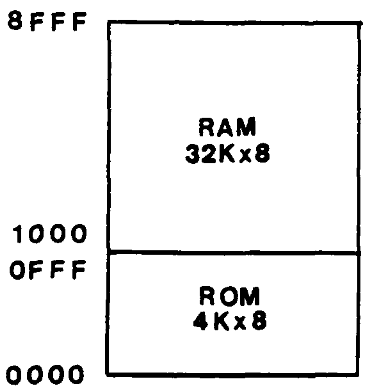

Figure 3-3 Developmental Configuration

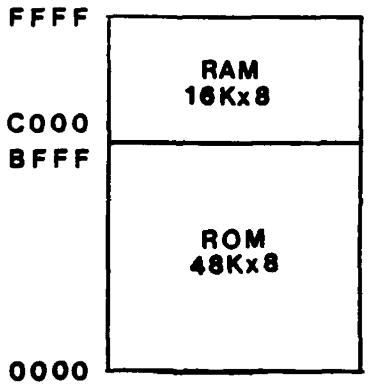

Figure 3-4 Large Fixed Applications

CHAPTER 4

4.0 INSTALLATION

4.1 Physical Requirements - The XQ/CP is physically designed to be mounted in a standard LSI-11 backplane. Three dual-height backplane slots are necessary. A fourth slot is necessary for the MDMA Controller if it is not already in the system. NOTE: The recommended configuration of the boards is to occupy four adjacent backplane slots. If this configuration is not possible, please consult the factory. There are no special physical requirements for any of the boards; all physical parameters of the XQ/CP meet LSI-11 standards.

4.2 Electrical Requirements - The XQ/CP uses two voltages: +5V DC and +12V DC. These are available from the LSI-11 backplane. All other voltages and signals are generated internally. The current requirements for each of the boards are listed in Table 4-1. These figures are the sums of the maximum supply currents of all circuits on each board. All three XQ/CP boards provide LSI-11 DMA grant continuity and interrupt grant continuity. There are two I/O paths that are normally connected to the XQ/CP. The first is a parallel path to the MDMA; this meets TTL electrical standards. The second is a serial path that meets one of the following Electronic Industries Association (EIA) standards: RS-232, RS-449 or

MIL-STD-188-114. The serial interface is installed by the factory according to user requirements, but it is field changeable.

	+5V DC	+12V DC
P-Board	2.26 A	272 mA
M-Board	3.26 A	960 mA
I-Board	2.72 A	0

Table 4-1 Current Requirements

4.3 Interconnection - The connection requirements of the XQ/CP have been described in Section 3.2 and have been illustrated in Figure 3-1. A summary of that description is tabulated in Table 4-2. Please refer to the previous discussion for more explanation.

FROM	TO	TYPE
MDMA (J1)	I-Board (J3)	40 Pin Flat Cable
P-Board (J1)	M-Board (J2)	40 Pin Flat Cable
M-Board (J1)	I-Board (J2)	40 Pin Flat Cable
P-Board (J2)	Serial Panel (M1)	26 Pin Flat Cable
P-Board (J3)	Serial Panel (M2)	26 Pin Flat Cable

Table 4-2 XQ/CP Connections

4.4 Options - All options of the XQ/CP are inplemented in one of four ways: (1) programmable read only memories (PROM), (2) printed circuit board jumpers, (3) component platform jumpers, or (4) switch settings. All options are initially set by the factory to default settings. Most applications will require no changes to these defaults; most field changes will only concern switch settings. Items (1) through (4) are listed in increasing probability and increasing ease to change. Table 4-3 summarizes all options available.

OPTION	CONFIGURATION OR SETTING
Memory mapping	1. Standard (default) 2. Specified by user
I/O Port Options	1. Standard (default) 2. Specified by user
Configuration*	1. With MDMA 2. Stand Alone
Serial Interface*	1. MIL-STD-188-114 2. RS-232 3. RS-422 4. RS-423
Subsystem Bus ID	1. 0 (default setting) 2. Switch settable
LSI-11 Base Address	1. 776200 (default setting) 2. Switch settable
LSI-11 Base Vector	1. 140 (default setting) 2. Switch settable

* Must be specified when ordering

Table 4-3 Summary of Options

4.4.1 PROM Options - Two functions are implemented by PROMs: Memory Mapping and I/O Mapping. These functions should not normally be altered since a complete restructuring of all XQ/CP software would be necessary. A detailed description of the operation of these PROM's is included in Section 6. Figure 4-1 and Table 4-4 summarize the memory and I/O addressing schemes.

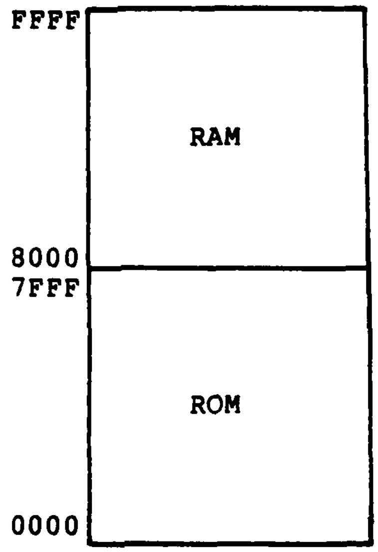

Figure 4-1 Standard Memory Map

DEVICE	DEVICE CODE OCTAL	HEXIDECIMAL
SIO Channel A - Data	000	00
SIO Channel A - Control	001	01
SIO Channel B - Data	002	02
SIO Channel B - Control	003	03
CTC Channel 0	020	10
CTC Channel 1	021	11
CTC Channel 2	022	12
CTC Channel 3	023	13
LEDS/DIP Switch	026	16
DMA Receive (-R) Channel	040	20
DMA Transmit (-T) Channel	042	22
DMA SIO-A Channel	044	24
DMA SIO-B Channel	046	26
DMA-R Data Register	050	28
DMA-T Data Register	052	2A
DMA-R Control Register	054	2C
DMA-T Control Register	056	2E
Baud Rate Generator	060	30
Serial Port	064	34

Table 4-4 Standard I/O Port Addresses

4.4.2 Printed Circuit Board Jumpers - The printed circuit board jumper options depend upon the type of RAMs and ROMs used and whether the XQ/CP is used with the MDMA or in stand alone mode. The jumpers are PC traces that are fabricated with both options connected. When the boards are assembled, one option is selected by cutting a trace. These jumpers are selected by the factory and do not normally need to be changed in the field. All jumpers are described in Table 4-5.

Board	Pin	Signal	Description
M	X01-1 X01-2 X01-3	+5V RADR12 ROMP23	For 2532 EPROMs, cut trace between 2 and 3. For 2564 EPROMs, cut trace between 1 and 3.
M	X02-1 X02-2 X02-3	ROMEN GND ROME	For 2532 and 2564 EPROMs, cut trace between 2 and 3.
M	X03-1 X03-2 X03-3	RAMEN GND RAME	For all 4116 RAMs, cut trace between 2 and 3.
M	X04-1 X04-2 X04-3	VM GND SEL	For standard memory map, cut trace between 1 and 3. For special memory map, cut trace between 2 and 3.
I	X01-1 X01-2	BCKB- BZCLK-	For operation with MDMA, leave as is For stand alone operation, cut trace between 1 and 2.
P	JMP1-1 JMP1-2	CLKD BZCLK-	For operation with MDMA, cut trace between 1 and 2. For operation with MDMA, leave as is.

Table 4-5 Printed Circuit Board Jumpers

4.4.3 Component Platform Jumpers- Component platforms are located on the P-Board. This determines which serial interface is available. The interfaces available are: RS-232, RS-449, or MIL-STD-188-114. There are four receive and four transmit platforms for each. These platforms are intalled by the factory to support the desired serial interface. If a field change is necessary, new platforms may be ordered from the factory or they can be fabricated as shown on Drawings 2600431-3. If RS-232 is required, U26, U29, U30, and U36 will be absent and U28 and U38 will be present. For all other interfaces, U28 and U38 are absent and U26, U29, U30, and U36 will be present.

4.4.4 Switch Settings- Switch settings determine addresses and vectors for the XQ/CP. They are given default settings are set by the factory (refer to Table 4-6). These default values are appropriate for systems where the XQ/CP is the only device on the Subsystem Interface Bus (SIB). If there are multiple devices on the SIB, the switch settings must be changed so that no two devices share the same vector or address. Table 4-7 will be useful in determining the proper switch settings. If the vector and address of the XQ/CP are changed, all factory supplied software will have to be recompiled with the correct address. The base address and address range of the MDMA may be altered by wire wrap jumpers on the MDMA board. Tables 4-6 and 4-7 reflect options based on the standard MDMA configuration. Refer to the *MDMA Maintenance Manual* if this type of change is necessary.

Option	Selectable Digits = X	Factory Setting	
SIB ID	X XXX	0 000	Octal Binary
LSI-11 Base Vector	XX0 XXXXX000	140 01100000	Octal Binary
LSI-11 Base Address	776XX0 1111111100XXXX0000	776200 1111111110010000000	Octal Binary

Table 4-6 Switch Selectable Values

Board	Switch	Signal	Switch On	Switch Off	Factory Default	Option
I I I	U60-1 U60-2 U60-3	ID03 ID02 ID01	0 0 0	1 1 1	ON - 0 ON - 0 ON - 0	SIB ID#
I I I I I	U60-4 U60-5 U60-6 U60-7 U60-8	VCT07 VCT06 VCT05 VCT04 VCT03	0 0 0 0 0	1 1 1 1 1	ON - 0 OFF - 1 OFF - 1 ON - 0 ON - 0	LSI-11 BASE Vector
I I I I	U65-1 U65-2 U65-3 U65-4	AJ7 AJ6 AJ5 AJ4	0 0 0 0	1 1 1 1	ON - 0 ON - 0 ON - 0 ON - 0	LSI-11 Base Address
I I I I	U65-5 U65-6 U65-7 U65-8	- - - -	- - - -	- - - -	- - - -	Not Used
P	UIO - 1 to 8	SW0- to SW7-	1	0	N/A	N/A

Table 4-7 Switch Positions

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CHAPTER 5 - PROGRAMMING

CHAPTER 5

5.0 PROGRAMMING

5.1 Protocol Processor - The XQ/CP is a fully programmable communications processor specifically designed for serial communication protocols. Protocol data is processed and moved into and out of LSI-11 "Host" memory via Direct Memory Access (DMA).

5.2 Microprocessor Programming - The XQ/CP Read-Only Memories (ROMs) contain an ACC Monitor Program implementing an inter-processor communications protocol. ACC Block Diagram 2700060 and Table 4-4 (I/O Ports Assignments) provide detailed information concerning the hardware configuration.

5.3 Host Programming - Host-based application programs within the LSI-11 access the serial paths by means of an ACC supplied device driver for each Host Operating System.

5.4 <u>Communication Registers</u> - The Monitor Program in the XQ/CP and the Host Device Driver interact via a set of Hardware Communication Registers (see Figure 5-1). Eight registers are available to the Host Device Driver:

Receive Control and Status Register	(RCSR)
Receive Data Register	(RDR)
Receive Address Register	(RAR)
Receive Word Count Register	(RWCR)
Transmit Control and Status Register	(TCSR)
Transmit Data Register	(TDR)
Transmit Address Register	(TAR)
Transmit Word Count Register	(TWCR)

5.5 <u>Contiguous Block of Addresses</u> - The registers of the Hardware Communication Register occupy a contiguous block of addresses on the LSI-11 QBUS, starting at an address determined by switch settings on the MDMA and XQ/CP circuit boards.

5.6 <u>Starting the DMA Transfer</u> - A DMA transfer is started when the Device Driver loads the data buffer starting address into the TAR, loads a 2's complement word count into the TWCR, and sets the GO bit in the TCSR. If a matching request has been issued by the XQ/CP based Inter-Processor Manager, the DMA hardware on the XQ/CP is activated and the transfer takes place. The microprocessor side of the transfer is set up by programming the appropriate Z80-DMA and by the use of the corresponding Z80 Control Register. These registers are detailed in the remainder of this section.

5.7 <u>Sense of Read and Write With Respect to the Communication Register</u> - The register descriptions in Table 5-1 through 5-4 are written from the point of view of the program using the registers. For example, sense of read and write of the MDMA TCSR and RCSR is from an LSI-11 program. The sense of read and write of the Z80 TCR and RCR is from a Z80 program.

Table 5-1 XQ/CP: MDMA RCSR (Receive Control and Status Register)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR	NXM	ZS3	ZS2	ZS1	ZS0	Z80 HALT	DBF	RDY	IEN	ADR 17	ADR 16		REC SIG	REC RES	GO
R	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R	W	W

BIT 0 GO — The GO bit. Setting this bit clears RDY and initiates a DMA transfer from the XQ/CP to the LSI-11 processor. Clearing this bit has no effect. GO will always read as zero.

BIT 1 REC RESET — The RECEIVE RESET bit. Setting this bit resets the receive DMA hardware. The entire XQ/CP to LSI-11 channel is reset. Clearing this bit has no effect. This bit will always read as zero.

BIT 2 REC SIGNAL — The RECEIVE SIGNAL bit. This bit is set to one upon completion of a receive DMA data transfer. If IEN is presently set, the LSI-11 is interrupted. RECEIVE SIGNAL is cleared upon reading the RCSR by the LSI-11. This bit is read-only and writing to this bit has no effect.

BIT 3 UNUSED — This bit is undefined and is reserved for future use. It is cleared upon system startup or reset.

BIT 4 ADR16 — This is ADDRESS BIT 16 for extended addressing operation. This bit is never modified by the XQ/CP. It is cleared upon system startup or reset.

BIT 5 ADR17 — This is ADDRESS BIT 17 for extended addressing operation. This bit is never modified by the XQ/CP. It is cleared upon system startup or reset.

BIT 6	IEN	The INTERRUPT ENABLE bit. The LSI-11 program sets this bit to allow the channel to request program interrupts and clears it to disallow interrupts. The channel only responds to interrupt polling cycles when this bit is on. It is cleared upon system startup or reset.
BIT 7	RDY	The READY bit. This bit is on when the channel is not in DMA mode. When the channel is ready, the Memory Address Register, the Word Count Register, and the Control and Status Register may be modified. This bit goes off when DMA mode is started by setting the GO bit. When DMA mode is active, setting this bit causes DMA to be stopped. Clearing this bit has no effect. This bit is set upon system startup or reset.
BIT 8	DBF	The DATA BUFFER FLAG bit. This bit indicates that the Receive Data Buffer contains a word and is ready to be read. This bit is allowed to be on only when the channel is in DMA mode (RDY = 0). DATA BUFFER FLAG is cleared when the Receive Data Buffer is read.
BIT 9	Z80 HALT	The Z80-CPU HALT bit. This bit indicates the halt state of the XQ/CP microprocessor. If the XQ/CP is halted, this bit will read as one. Otherwise, this bit will read as zero. This is a read-only bit and writing to this bit has no effect.
BIT 10	ZS0	This is Z80 STATUS BIT 0. This bit and the following Z80 Status Bits are user defined status bits passed from the XQ/CP program to the LSI-11 program. These bits are read-only and writing to these bits has no effect.
BIT 11	ZS1	This is Z80 STATUS BIT 1. See ZS0.
BIT 12	ZS2	This is Z80 STATUS BIT 2. See ZS0.
BIT 13	ZS3	This is Z80 STATUS BIT 3. See ZS0.

BIT 14	NXM	The NONEXISTENT MEMORY ERROR bit. This bit being set indicates that DMA was attempted to an LSI-11 address which did not respond. This bit is set by the MDMA and is tested and reset by the LSI-11 program.
BIT 15	ERR	The COMPOSITE ERROR bit. This bit is the logical OR of all error bits. Currently the only defined error is NONEXISTENT MEMORY ERROR. The ERROR bit is reset by resetting all other error bits. This bit is read-only. It is cleared upon system startup or reset.

Table 5-2 XQ/CP: MDMA TCSR (Transmit Control and Status Register)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR	NXM	PS3	PS2	PS1	PS0		DBF	RDY	IEN	ADR 17	ADR 16	Z80 RES	XMT SIG	XMT RES	GO
R	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R	W	W

BIT 0 GO

The GO bit. Setting this bit causes RDY to be reset to zero and initiates a DMA transfer from the LSI-11 processor to the XQ/CP. Clearing this bit has no effect. GO will always read as zero.

BIT 1 TRANS RESET

The TRANSMIT RESET bit. Setting this bit resets the transmit DMA hardware. The entire LSI-11 to XQ/CP channel is reset. This bit will always read as zero. Clearing this bit has no effect.

BIT 2 TRANS SIGNAL

The TRANSMIT SIGNAL bit. Setting this bit interrupts the XQ/CP. This bit will always read as zero. Clearing this bit has no effect.

BIT 3 Z80 RESET

The Z80 RESET bit. Setting this bit resets the Z80 hardware in the XQ/CP and causes the Z80 CPU to restart at location zero. Clearing this bit has no effect. This bit will always read as zero.

BIT 4 ADR16

This is ADDRESS BIT 16 for extended addressing operation. It is cleared upon system startup or reset.

BIT 5 ADR17

This is ADDRESS BIT 17 for extended addressing operation. It is cleared upon system startup or reset.

BIT 6 IEN

The INTERRUPT ENABLE bit. The LSI-11 program sets this bit to allow the channel to request program interrupts and clears it to disallow interrupts. The channel only responds to interrupt polling cycles when this bit is on. It is cleared upon system startup or reset.

BIT 7 RDY

The READY bit. This bit has a value of one when the channel is not in DMA

mode. When the channel is ready the Memory Address Register, the Word Counter Register, and the Control and Status Register may be modified. This bit is cleared when DMA mode is started by setting the GO bit. When DMA mode is active, setting RDY causes DMA to be stopped. Clearing this bit has no effect. It is set upon system startup or reset.

BIT 8	DBF	The DATA BUFFER FLAG bit. This bit indicates that the Transmit Data Buffer is empty and is ready to accept a new word. This bit has a value of one only when the channel is in DMA mode (RDY = 0). DATA BUFFER FLAG is cleared when the Transmit Data Buffer is written.
BIT 9	UNUSED	This bit is always read as a zero.
BIT 10	PS0	This is PROCESSOR STATUS BIT 0. This bit and the following Processor Status bits are user defined status bits that are passed from the LSI-11 program to the XQ/CP program. These bits may be set or cleared as required by the LSI-11 program. It is cleared upon system startup or reset.
BIT 11	PS1	This is PROCESSOR STATUS BIT 1. See PS0.
BIT 12	PS2	This is PROCESSOR STATUS BIT 2. See PS0.
BIT 13	PS2	This is PROCESSOR STATUS BIT 3. See PS0.
BIT 14	NXM	The NONEXISTENT MEMORY ERROR bit. This bit has a value of one when DMA was attempted to an LSI-11 address which did not respond. This bit is set by the MDMA and is tested and cleared by the LSI-11 program.
BIT 15	ERR	The COMPOSITE ERROR bit. This bit is the logical OR of all error bits. Currently the only defined error is NONEXISTENT MEMORY ERROR. The ERROR bit is reset by resetting all other error bits. This bit is read-only. It is cleared upon system startup or reset.

Table 5-3 XQ/CP: Z80 RCR(Z80 Receiver Control Register)

7	6	5	4	3	2	1	0
RDY	XMT SIG	ODD	DBF	PS3	PS2	PS1	PS0
R	R	R	R	R	R	R	R

BIT 0 PS0	This is PROCESSOR STATUS BIT 0. This bit and the following Processor Status Bits are user defined status bits passed from the LSI-11 program to the XQ/CP program. They are read-only.
BIT 1 PS1	This is PROCESSOR STATUS BIT 1. See PS0.
BIT 2 PS2	This is PROCESSOR STATUS BIT 2. See PS0.
BIT 3 PS3	This is PROCESSOR STATUS BIT 3. See PS0.
BIT 4 DBF	The DATA BUFFER FLAG bit. This bit being set inidicates that the MDMA's Transmit Data Buffer is empty.
BIT 5 ODD	The ODD BYTE bit. This bit being set indicates that an odd number of bytes have been transferred to the Z80 Receive Data Buffer. Completed transfers should always have an even number of bytes. This bit is read-only. It is cleared upon system startup or reset.
BIT 6 TRANS SIGNAL	The MDMA TRANSMIT SIGNAL bit. When the LSI-11 sets this bit channel 3 of the Z80-CTC is strobed. If the CTC channel 3 has been programmed with a count of 1, this will cause an interrupt of the Z80-CPU. This bit will remain a one until after the Z80-RCR is read. This bit is read-only.
BIT 7 RDY	The READY bit. This bit being set indicates that the LSI-11 to XQ/CP channel is ready for a DMA block transfer. This bit being cleared indicates that a DMA transfer is in progress. This bit is read-only.

Table 5-4 XQ/CP: Z80 TCR (Z80 Transmit Control Register)

7	6	5	4	3	2	1	0
RDY	REC SIG	ODD		ZS3	ZS2	ZS1	ZS0
R	W	R		R/W	R/W	R/W	R/W

BIT 0 ZS0 — This is Z80 STATUS BIT 0. This bit and the following Z80 Status bits are user defined status bits passed from the XQ/CP program to the LSI-11 program. These bits are read/write.

BIT 1 ZS1 — This is Z80 STATUS BIT 1. See ZS0.

BIT 2 ZS2 — This is Z80 STATUS BIT 2. See ZS0.

BIT 3 ZS3 — This is Z80 STATUS BIT 3. See ZS0.

BIT 4 DBF — The DATA BUFFER FLAG. This bit indicates that the Receive Data Buffer contains a word and is ready to be read. DATA BUFFER STATUS is cleared when the Receive Data Buffer is read.

BIT 5 ODD — The ODD BYTE Bit. This bit being set indicates that an odd number of bytes have been transferred to the MDMA Receive Data Buffer. Completed transfers should always have an even number of bytes. This bit is read-only. It is cleared upon system startup or reset.

BIT 6 REC SIGNAL — The MDMA's RECEIVE SIGNAL bit. Setting this bit interrupts the LSI-11 program. Clearing this bit has no effect. This bit is write-only and will always be read as zero.

BIT 7 RDY — The READY bit. This bit being set indicates that the XQ/CP to LSI-11 channel is ready for a DMA block transfer. This bit being zeroed indicates that the channel is active in DMA mode. This bit is read-only.

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CHAPTER 6 - DETAILED DESCRIPTION

CHAPTER 6

6.0 DETAILED DESCRIPTION

6.1 <u>Drawing References for Circuit Descriptions</u> - This chapter contains circuit descriptions of each XQ/CP board. Each section in this chapter describes the circuits on a drawing by drawing basis. Please refer to the drawings as the discussion proceeds. Coordinate numbers on the drawings are used to help locate signals or circuits. These are letter number pairs (e.g. A8) that are marked on the edge of the drawing page. Signal names indicate polarity: An active low signal is followed by a minus, otherwise the signal is active high. Active low signals are drawn with bubble outputs and inputs.

6.2 <u>Processor Board</u> - The logic drawings for the Processor Board are Pages 1 through 3, Drawing 2600431.

6.2.1 <u>Processor Board Drawing, Page 1</u> - Page 1 contains the major Z80 components. The Z80-CPU, both Z80 DMA's, the Z80-SIO, the Z80-CTC, and the baud rate generator are all on this page. These components connect to the Z80 Bus according to Zilog specifications. Consult Zilog technical manuals for component operation and programming. In the XQ/CP, a Z80A-CPU is used. An external reset signal is synchronized to generate the CPU's reset signal. This signal resets the program counter to zero so that orderly execution will begin after a reset. Each Z80-DMA can control one serial channel of the Z80-SIO. U17 monitors SIORDYA from SIO Channel A; U16 monitors SIORDYB from SIO Channel B. When programmed and enabled, the DMA control of the SIO channels will allow higher speed serial transfers than when the SIO is directly controlled by the CPU. The outputs of the SIO channels go to serial line drivers located on page 3 for RS-449 and MIL-STD-188-114 and on page 1

for RS-232. The drivers for the unimplemented serial interfaces are not mounted on the board. The Z80-CTC provides counter-timer functions. Channel 3 is intended to provide a mechanism for external interrupts. CTC Channel 3 is loaded with a count of 1. When TSIGNAL goes active, it clocks the channel to zero. This creates an interrupt. A baud rate generator, the K1135A, is programmable by the CPU for baud rates from 50 baud to 19.2 kilobaud. A component platform, U07, is provided to jumper either output of the baud rate generator or modem supplied clocks to any of the serial clocks. This provides flexibility in choice of clocks. The last elements on page 1 are the power converter and regulator for -5V and -12V.

6.2.2 Processor Board Drawing, Page 2 - Page 2 contains off-board Z80 Bus connections, I/O Port decoding, and the stand alone clock. U24 and U34 are 74LS245 transceivers for the Z80 Bus address bits. U33 is the transceiver for the data bits. U23 and U27 buffer control signals. U22 is a 74S471 ROM containing a table of ports. These are listed in Table 4-4. These outputs are used to enable various Z80 Bus I/O devices. One of these addresses is a DIP switch register for reading user supplied data. The same I/O port address is used to write to a register that drives eight LED's that are mounted on the edge of the P-Board. The final circuit on the page is a 4 mHz clock generator for stand alone operation. At coordinates D5, the jumper is shown that enables the clock selection. The output of this jumper is the source for both the MOS clock driver, PCLKM, and the TTL driver, PCLKT.

6.2.3 Processor Board Drawing, Page 3 - Page 3 contains the drivers and receivers for the serial interface. The drawing is organized top to bottom for Channel 0 to Channel 1 and left to right for receivers and drivers. This organization is clearly marked on the drawing. The receivers are 3486 RS-422/RS-423 Line Receivers. With external components these receivers can receive RS-232 and MIL-STD-188-114. Component platforms have been provided to accomplish this. They are drawn in A5 through A8. The drivers are 3691 RS-422/RS-423 Line Drivers. Component platforms have been provided to support the different serial line specifications. When using this drawing it should be observed that the signal names ending in H and L are derived from the + and - inputs or outputs of the receiver and drivers; H and L do not correspond to the A and B sides of the EIA serial signals. Please consult the chart on page 3 of the P-Board drawing for this correspondence.

6.3 Memory Board - The logic drawings for the Memory Board are drawing 2600430, pages 1 and 2.

6.3.1 Memory Board Drawing, Page 1 - Page 1 contains the ROM circuits. The ROM types may be either 2564 or 2532. The board is populated with eight 28 pin sockets and will accept either type of ROM. If 2532 ROMs are used, pin 1 is plugged into pin 3 of the socket. The address blocks that the ROMs respond to are determined by the chip enables, CS0- to CS7-, with CS0- as the lowest address. This address decoding is done by U13 at A7. The other circuit elements on this page are Z80 Bus address receivers that buffer address bits for the M-Board.

6.3.2 Memory Board Drawing, Page 2 - Page 2 of 2600430 contains 32K bytes of RAM. The memory circuits are 4116 Dynamic RAMs. Refresh is provided by the Z80-CPU. Control circuitry to generate the proper row (RAS-) and column (CAS0- and CAS1-) strobe timing is shown on this page. This timing is accomplished by multiplexing the Z80 Bus address signals in U40 and U41 (C8). During a memory cycle, the Z80 device controlling the bus will assert BZMREQ- which will set ADRSEL (see Figure 6-1). This selects BZADR07-13 as the column address bits. This selection occurs after the row address bits have been asserted for approximately 110ns. RAS- is asserted starting with MREQ and ending when PCQ2 is asserted. Refer to Figure 6-1 for the timing of PCQ1 and PCQ2. The column address strobes become active after the delays provided by the 74LS04s generating MAS2 at C6. Figure 6-1 shows the timing for a CPU M1 cycle, an instruction fetch. The circuit at B2-B3 generates a wait cycle during an instruction fetch. The types of RAMs and ROMs currently available require the generation of this wait cycle. A jumper disable of this circuit (ROME to GND or RAME to GND at B3) has been provided if faster memory circuits become available. Figure 6-1 shows the generation of this wait cycle.

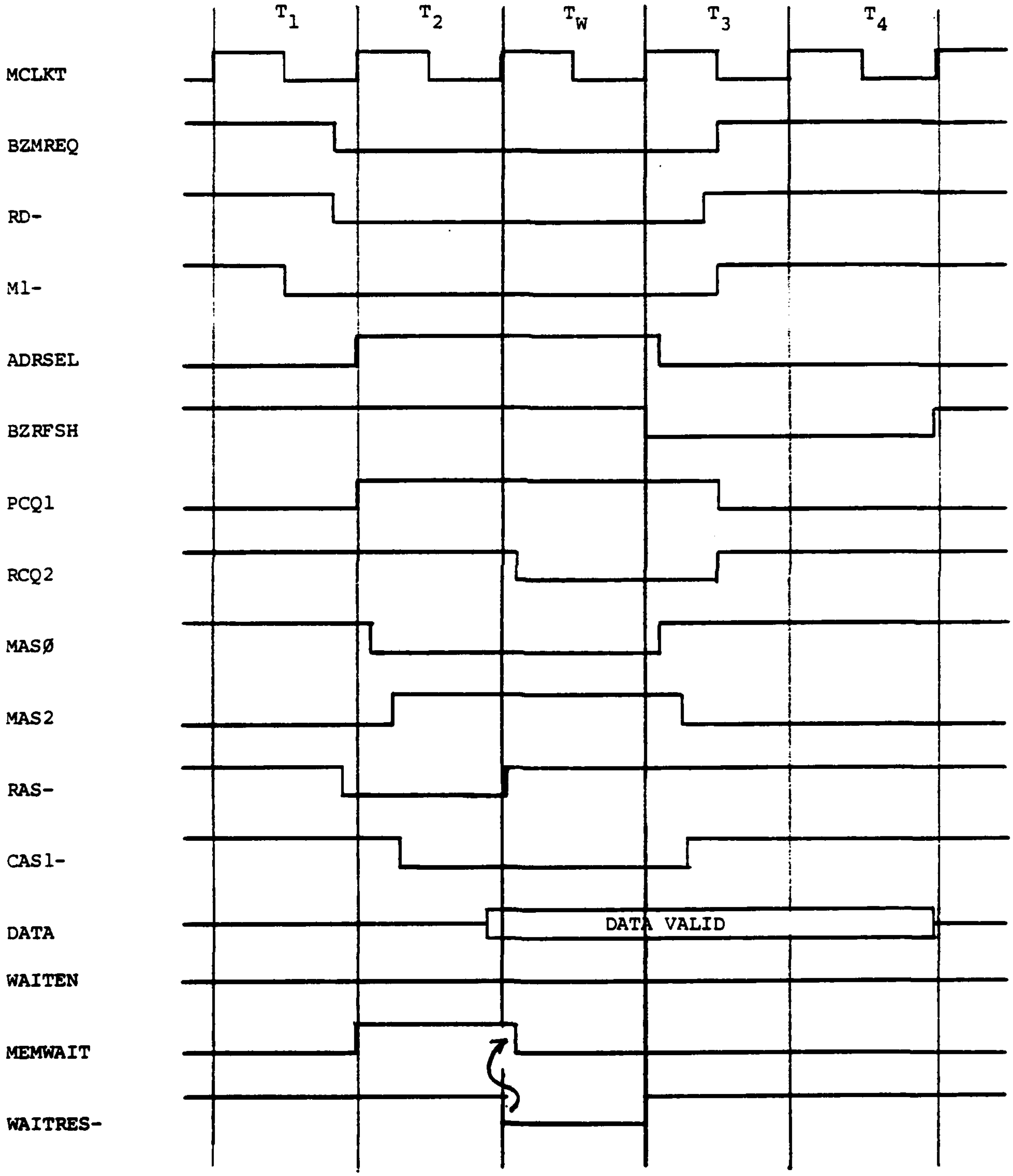

FIGURE 6-1 RAM ACCESS TIMING DIAGRAM

6.4 Interface Board - The I-Board drawings are on 2600429 pages 1-5.

6.4.1 Interface Board, Page 1 - Page 1 contains the Z80 receive DMA circuits. The main elements on this page are the Z80-DMA, a buffer for the control register bits (U23 at B5), the data registers that receive 16 bit LSI-Bus data and put 8 bit data on the Z80 Bus, and control circuits. The key to understanding the receive circuits is in the control circuits. When a word is available to the 16 bit data register, TDBCK- is generated. This clocks the data into U02 and U03 and also clocks both J-K flip-flops of U39. This sets TDBL and TDBU (see Figure 6-2 on next page). With these signals active DMARRDY will be set on the next active edge of ICLKT-. Since TDBLOE- was active for the clock prior to the setting of DMARRDY, the eight least significant bits of data will be clocked into U01. Additionally, TDBL is reset causing TDBLOE- to go inactive and TDBU to go active. The Z80 DMA will respond to DMARRDY if it has been properly programmed and enabled. It will request a Z80 Bus transfer. When granted the bus, the DMA will read the 8 bit register, causing ZDBOE- to go active (D4). This will toggle DMARRDY on the next clock. Since a byte is still in the register, TDBU is still active. This will cause DMARRDY to go active on the following clock which strobes the upper byte into the 8 bit register and re-enables the Z80 DMA. The DMA will go through another bus acquisition and data transfer cycle completing the 16 bit transfer. The final circuit on this page is to generate ZRCYL, a single clock version of ZDBOE. This is done with a D flip-flop, U34 at C7. The Q output is brought to an AND gate with the inverted D input to create ZRCYL (see Figure 6-3 on next page). This scheme is also used to generate ZTCYL on page 3-C6, RSIGSET on page 3-D5, and CLRTSIG on page 5-C1.

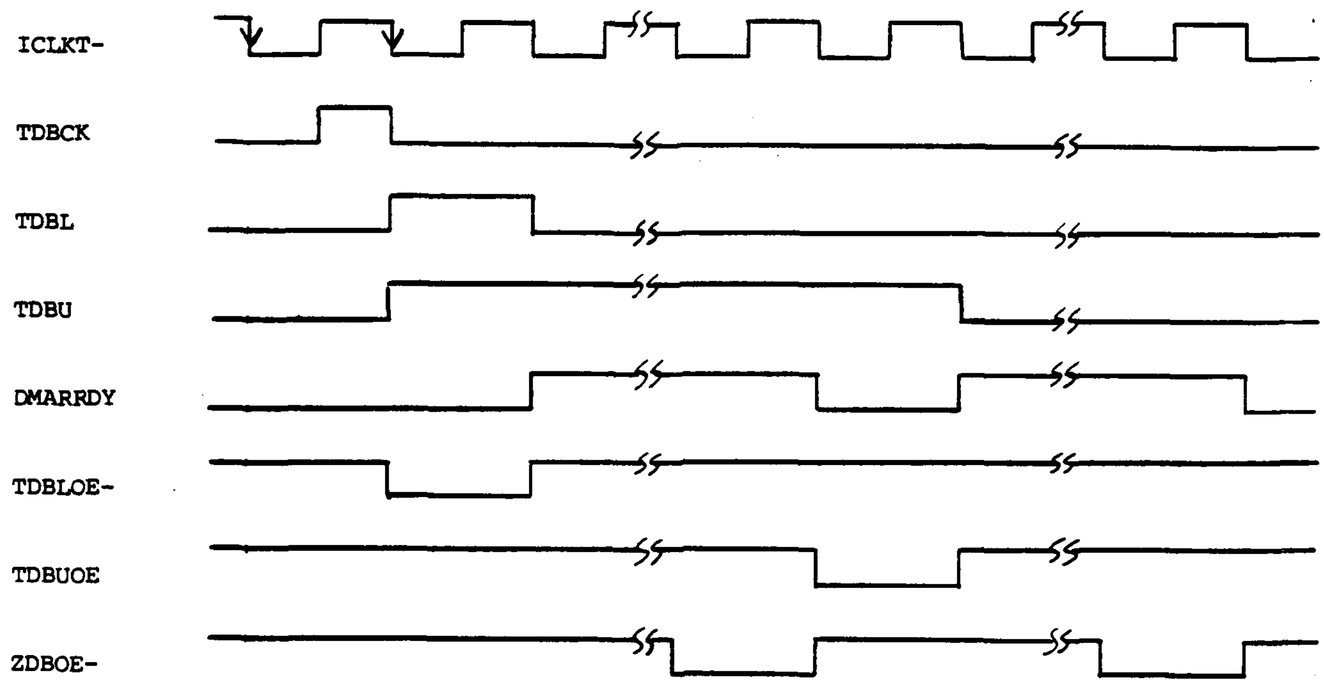

FIGURE 6-2 LSI-BUS TO Z8Ø-BUS DMA TRANSFER
TIMING DIAGRAM

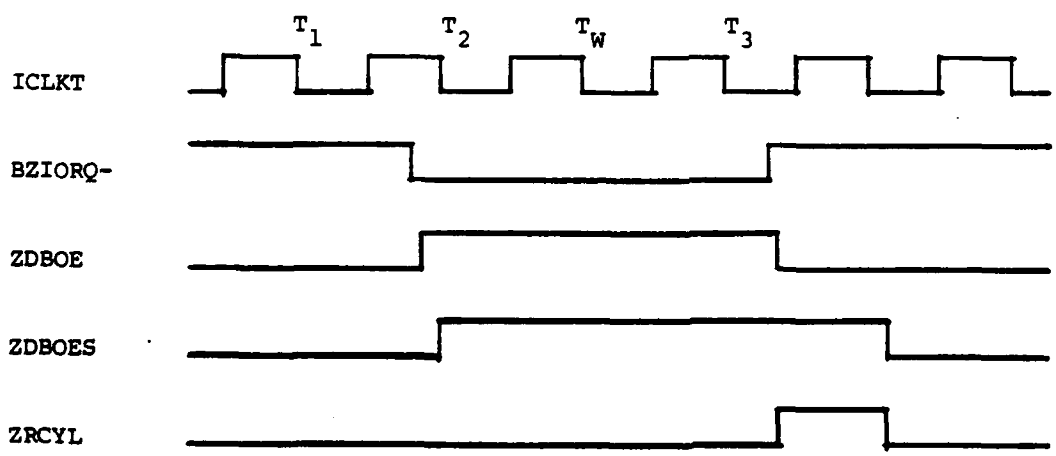

FIGURE 6-3 SINGLE CLOCK VERSION OF
I/O REQUEST

6.4.2 <u>Interface Board, Page 2</u> - Page 2 of Drawing 2600429 contains the SIB registers. The registers are implemented using 4x4 Register Files, 74LS670. The clocks, output control, and address bits are generated on page 4 from the SIB control signals, and will be discussed below. The other two elements on this page are two 8304B Transceivers which buffer the SIB data bits from an internal three state bus, DX00 to DX15. Note that the SIB bits begin with X; the glossary refers to the Subsystem Interface Bus as the X-Bus. This bus is used by the communications registers shown on page 2 and by the data and control registers shown on other pages. Interface Board, Page 3 - Page 3 shows the Z80 transmit DMA circuits. A transfer sequence would begin by programming the DMA, U53, and enabling it. If the GO bit has been set DMATRDY (at C5) will be active and the Z80 DMA will request a bus acquisition. When the bus has been granted, it will write a byte into the 8 bit register, U04 at B4. The first clock after the data has been latched will cause ZTFULL to go active and turn off DMATRDY (refer to Figure 6.4 on next page). RLFULL will be set on the next clock causing the data to be latched in the lower 8 bits of the 16 bit data register, U05. ZTFULL also changes on this clock since ZTFULL had been active and RDBF-(D2) is still high. This results in DMATRDY going ready so that another byte is obtained by the Z80 DMA. This byte will set RUFULL, clocking the data into the upper 8 bits of the register, U06. When the word is read from the 16 bit register, RDBE- is strobed which will reset the remaining signals that are active. The Z80 DMA will be free to transfer another byte into U04 as soon as ZTFULL goes to zero. This may be before the 16 bit transfer is accomplished and thus block transfers are efficiently pipelined. The remaining circuits on this page include the control register U14 at C4 and its buffer U15, an I/O port decoder ROM (U54 at B7) and an interrupt mechanism. An interrupt to the LSI-11 QBUS is conveyed by the MDMA when RSIGNAL is set (D4). The control of this signal is critical in order to prevent a loss of RSIGNAL while the control register is being read. The timing of all possible cases is given in Figure 6-5 on page 6-9.

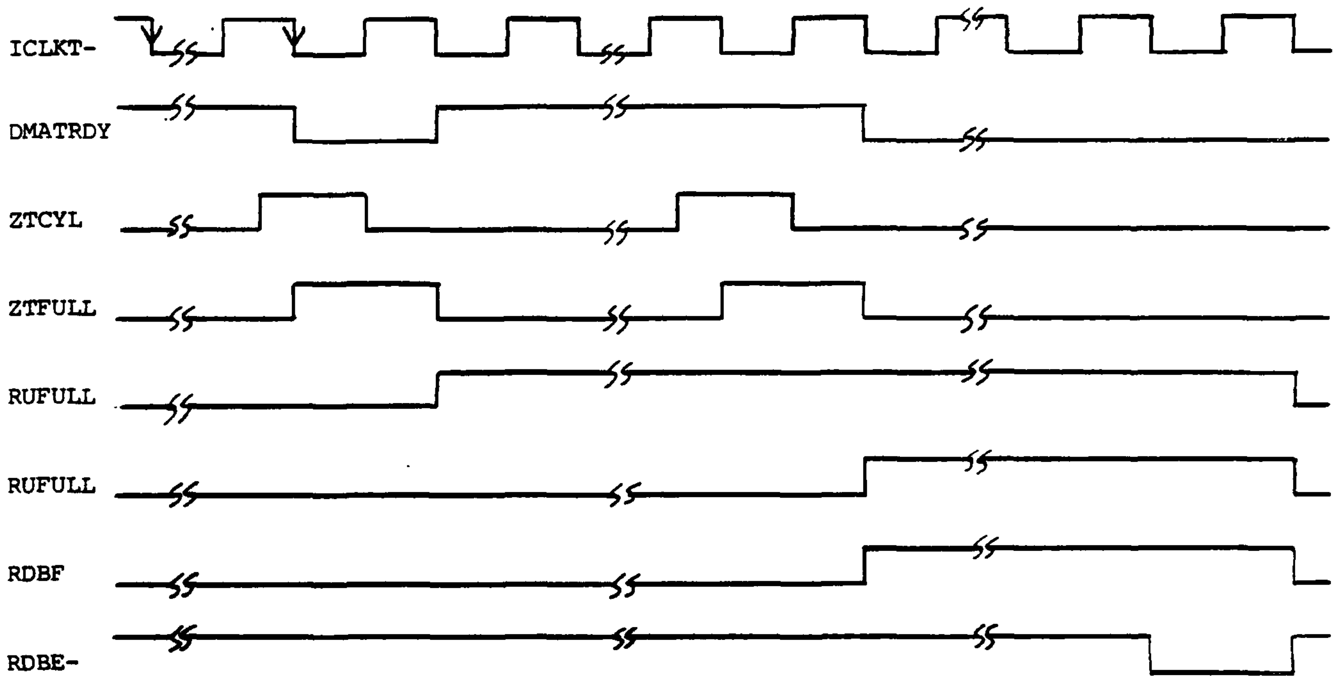

FIGURE 6-4 Z8Ø-BUS TO LSI-BUS DMA TRANSFER
TIMING DIAGRAM

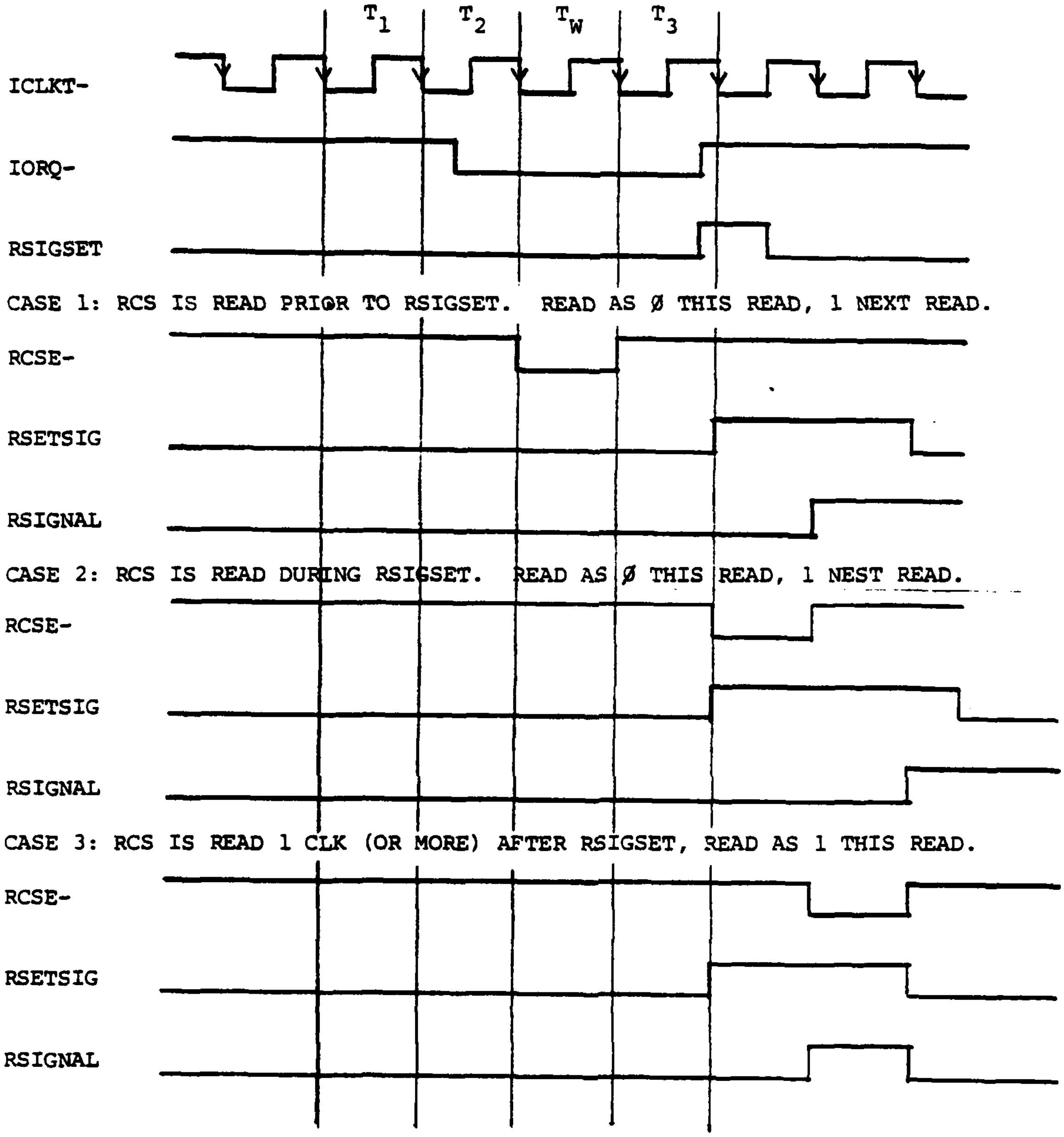

FIGURE 6-5 RSIGNAL TIMING DIAGRAM

6.4.3 Interface Board, Page 4 - Page 4 of the I-Board drawings contains circuits that are used to interface to the SIB. At C8 there is a DIP switch that selects address bits for a 25LS2521 comparator. If the SIB address bits are the same, SEL- goes active. This signal is used as an enable on U51, U19, and U21 (D5 through B5). These decoders generate vector enables, communication register output enables and strobes. The last decoder, U57, decodes function bits to determine what kind of operation to perform. The two J-K flip flops in B7 and A7 generate interrupts to the LSI-11 through the SIB. RIRDY- and TIRDY- cause XBRDY-. XBRDY- is the MDMA's polling condition that will cause it to generate an interrupt to the LSI-11. TIRDY- is generated when bit 7 of the control register is set (READY) after the transmit GO bit is on. This is normally done at the end of a data block transfer, but may also be done under LSI-II program control. RIRDY- is generated under similar circumstances and can also be generated by setting RSIGSET, the Z80 to LSI-11 signal term. The remaining circuit elements on this page are the buffering of the SIB clock signal, DCKB-, and the generation of the different reset signals.

6.4.4 Interface Board, Page 5 - Page 5 contains the SIB control and status registers. The bits are latched in 74LS174 registers and driven onto the three state DX data lines by 74LS244 buffers. Clocking and output controls are from the decoders on page 4. The control signal that generates a Z80 interrupt is TSIGNAL. The timing problems are similar to those for RSIGNAL; all cases of a TSIGNAL interrupt are shown in Figure 6-6. Please note that both RSIGNAL and TSIGNAL remain active until the side that has been interrupted reads the control register. The control register read resets the bit to zero.

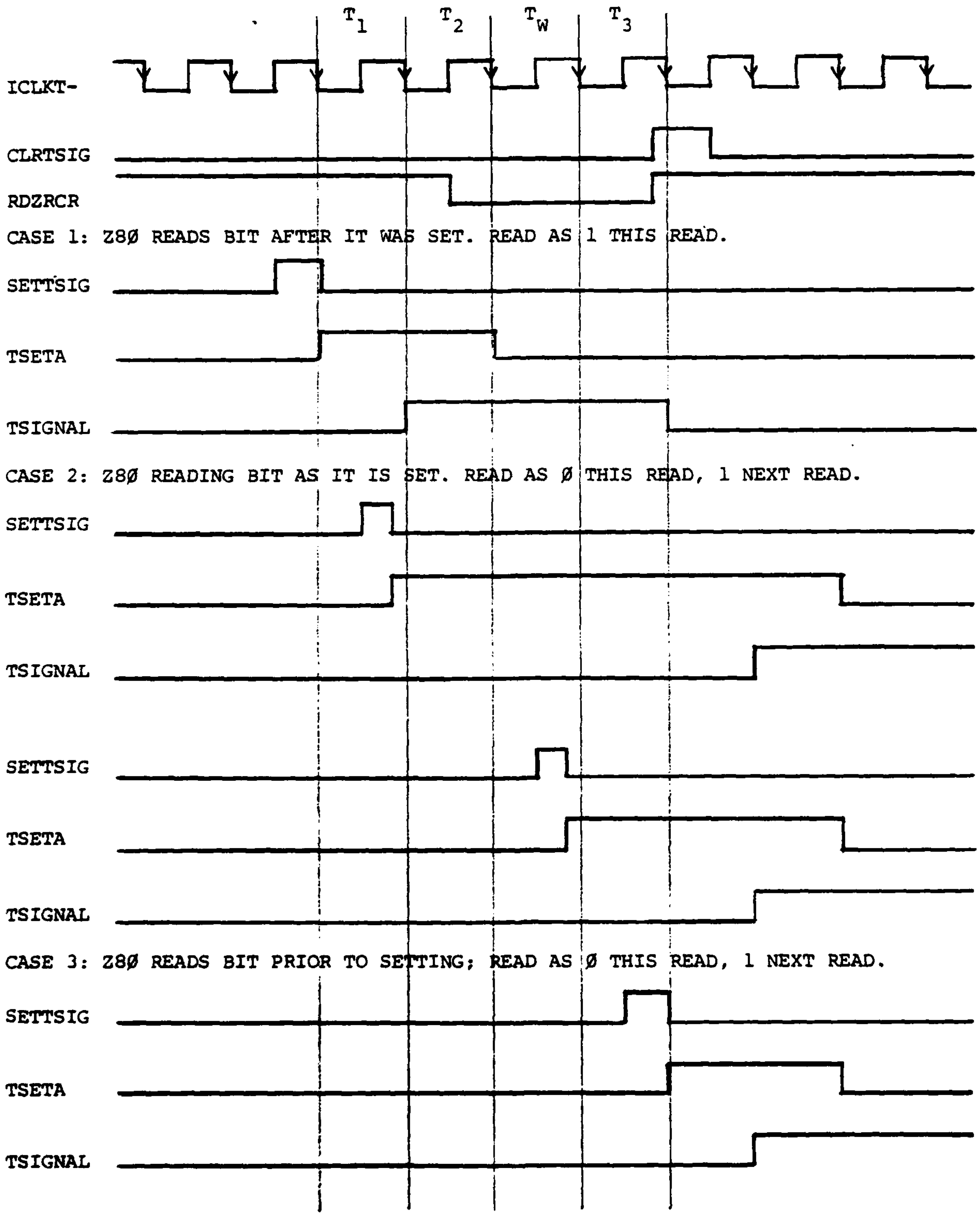

FIGURE 6-6 TSIGNAL TIMING DIAGRAM

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CHAPTER 7 - GLOSSARY

CHAPTER 7

7.0 GLOSSARY

4MCLK	4 Megahertz Clock
8MCLK	8 Megahertz Clock
A0	RAM Address Bit 0 (Attenuated)
A0D	RAM Address Bit 0 (Unattenuated)
A1	RAM Address Bit 1 (Attenuated)
A1D	RAM Address Bit 1 (Unattenuated)
A2	RAM Address Bit 2 (Attenuated)
A1D	RAM Address Bit 2 (Unattenuated)
A3	RAM Address Bit 3 (Attenuated)
A3D	RAM Address Bit 3 (Unattenuated)
A4	RAM Address Bit 4 (Attenuated)
A4D	RAM Address Bit 4 (Unattenuated)
A5	RAM Address Bit 5 (Attenuated)
A5D	RAM Address Bit 5 (Unattenuated)
A6	RAM Address Bit 6 (Attenuated)
A6D	RAM Address Bit 6 (Unattenuated)
AB1	MSIB Address Bit 1
AB2	MSIB Address Bit 2
AB3	MSIB Address Bit 3
ADRSEL	MDMA Address Select
AJ4	Address Jumper Bit 4
AJ5	Address Jumber Bit 5
AJ6	Address Jumper Bit 6
AJ7	Address Jumber Bit 7
AL12	Address Latch Bit 12
AL13	Address Latch Bit 13
AL14	Address Latch Bit 14
AL15	Address Latch Bit 15
BA0-	Bus Acknowledge 0
BA1-	Bus Acknowledge 1
BA2-	Bus Acknowledge 2
BAO-	Bus Acknowledge Out
BCKB-	MSIB Clock
BDMG-	LSI-11 Bus DMA Grant
BIAK-	LSI-11 Bus Interrupt Acknowledge
BINTACK-	Z80 Bus Interrupt Acknowledge
BLOCK-	Block TSIGNAL from setting
BRGEN	Baud Rate Generator Enable
BZADR00	Buffered Z80 Address Bit 00
BZADR01	Buffered Z80 Address Bit 01
BZADR02	Buffered Z80 Address Bit 02
BZADR03	Buffered Z80 Address Bit 03
BZADR04	Buffered Z80 Address Bit 04
BZADR05	Buffered Z80 Address Bit 05
BZADR06	Buffered Z80 Address Bit 06
BZADR07	Buffered Z80 Address Bit 07

BZADR08	Buffered Z80 Address Bit 08
BZADR09	Buffered Z80 Address Bit 09
BZADR10	Buffered Z80 Address Bit 10
BZADR11	Buffered Z80 Address Bit 11
BZADR12	Buffered Z80 Address Bit 12
BZADR13	Buffered Z80 Address Bit 13
BZADR14	Buffered Z80 Address Bit 14
BZADR15	Buffered Z80 Address Bit 15
BZBUSRQ-	Buffered Z80 Bus Request
BZCLK	Buffered Z80 Clock
BZDAT0	Buffered Z80 Bus Data Bit 0
BZDAT1	Buffered Z80 Bus Data Bit 1
BZDAT2	Buffered Z80 Bus Data Bit 2
BZDAT3	Buffered Z80 Bus Data Bit 3
BZDAT4	Buffered Z80 Bus Data Bit 4
BZDAT5	Buffered Z80 Bus Data Bit 5
BZDAT6	Buffered Z80 Bus Data Bit 6
BZDAT7	Buffered Z80 Bus Data Bit 7
BZEN-	Buffered Z80 Bus Enable
BZEN1-	Buffered Z80 Bus Enable 1
BZEN2-	Buffered Z80 Bus Enable 2
BZEN3-	Buffered Z80 Bus Enable 3
BZHALT	Buffered Z80 Bus Halt Bit
BZIN-	Buffered Z80 Bus Input Enable
BZINT-	Buffered Z80 Bus Interrupt
BZIORQ-	Buffered Z80 Bus Input/Output Request
BZM1	Buffered Z80 Bus Machine Cycle 1
BZMREQ-	Buffered Z80 Bus Memory Request
BZRD-	Buffered Z80 Bus Read Cycle
BZRFSH-	Buffered Z80 Bus Refresh Cycle
BZWR-	Buffered Z80 Bus Write Cycle
CAS0-	Column Address Strobe 0 (Attenuated)
CAS1-	Column Address Strobe 1 (Attenuated)
CASD0-	Column Address Strobe 0 (Unattenuated)
CASD1-	Column Address Strobe 0 (Unattenuated)
CLKD	D-Input to Clock Flip-flop
CLRTSIG	Clear Transmit Signal
CS0-	ROM Chip Select 0
CS1-	ROM Chip Select 1
CS2-	ROM Chip Select 2
CS3-	ROM Chip Select 3
CS4-	ROM Chip Select 4
CS5-	ROM Chip Select 5
CS6-	ROM Chip Select 6
CS7-	ROM Chip Select 7
CTCEN-	CTC Chip Enable
CTS0-	Clear to Send Channel 0, Active Low
CTS0H	Clear to Send Channel 0, + Term to Receive
CTS0HI	Clear to Send Channel 0, + Term on Input Connector
CTS0L	Clear to Send Channel 0, - Term to Receiver
CTS0LI	Clear to Send Channel 0, - Term on Input Connector
CTS1-	Clear to Send Channel 1, Active Low
CTS1H	Clear to Send Channel 1, - Term to Receiver
CTS1HI	Clear to Send Channel 1, - Term on Input Connector
CTS1L	Clear to Send Channel 1, - Term to Receiver
CTS1LI	Clear to Send Channel 1, - Term on Input Connector

DCD0	Data Carrier Detect Channel 0
DCD0H	Data Carrier Detect Channel 0, + Term to Receiver
DCD0HI	Data Carrier Detect Channel 0, + Term on Input Connector
DCD0L	Data Carrier Detect Channel 0, - Term to Receiver
DCD1-	Data Carrier Detect Channel 1, Active Low
DCD1H	Data Carrier Detect Channel 1, + Term to Receiver
DCD1HI	Data Carrier Detect Channel 1, + Term on Input Connector
DCD1L	Data Carrier Detect Channel 1, - Term to Receiver
DCD1LI	Data Carrier Detect Channel 1, - Term on Input Connector
DI0	RAM Data In Bit 0
DI1	RAM Data In Bit 1
DI2	RAM Data In Bit 2
DI3	RAM Data In Bit 3
DI4	RAM Data In Bit 4
DI5	RAM Data In Bit 5
DI6	RAM Data In Bit 6
DI7	RAM Data In Bit 7
DMAREN-	DMA Receive Channel Chip Enable
DMARRDY	DMA Receive Channel Ready
DMARRDY-	DMA Receive Channel Ready, Active Low
DMASAEN-	DMA for SIO Channel A, Chip Enable
DMASBEN-	DMA for SIO Channel B, Chip Enable
DMATEN-	DMA Transmit Channel Enable
DMATRDY	DMA Transmit Channel Ready
DO0	RAM Data Out Bit 0
DO1	RAM Data Out Bit 1
DO2	RAM Data Out Bit 2
DO3	RAM Data Out Bit 3
DO4	RAM Data Out Bit 4
DO5	RAM Data Out Bit 5
DO6	RAM Data Out Bit 6
DO7	RAM Data Out Bit 7
DSR0H	Data Set Ready Channel 0, + Term from Driver
DSR0HI	Data Set Ready Channel 0, + Term on Output Connector
DSR0L	Data Set Ready Channel 0, - Term from Driver
DSR0HI	Data Set Ready Channel 0, - Term on Output Connector
DSR1H	Data Set Ready Channel 1, + Term from Driver
DSR1HI	Data Set Ready Channel 1, + Term on Output Connector
DSR1L	Data Set Ready Channel 1, - Term from Driver
DSR1LI	Data Set Ready Channel 1, - Term on Output Connector
DTR0H	Data Terminal Ready Channel 0, + Term from Driver
DTR0HO	Data Terminal Ready Channel 0, + Term on Output Connector
DTR0L	Data Terminal Ready Channel 0, - Term from Driver
DTR0LO	Data Terminal Ready Channel 0, - Term on Output Connector
DTR1-	Date Terminal Ready Channel 1, Active Low
DTR1H	Data Terminal Ready Channel 1, + Term from Driver
DTR1HO	Data Terminal Ready Channel 1, + Term on Output Connector
DTR1L	Data Terminal Ready Channel 1, - Term from Driver
DTR1LO	Data Terminal Ready Channel 1, - Term on Output Connector
DX00	DX Bus Bit 00
DX01	DX Bus Bit 01
DX02	DX Bus Bit 02
DX03	DX Bus Bit 03
DX04	DX Bus Bit 04
DX05	DX Bus Bit 05
DX06	DX Bus Bit 06

DX07	DX Bus Bit 07
DX08	DX Bus Bit 08
DX09	DX Bus Bit 09
DX10	DX Bus Bit 10
DX11	DX Bus Bit 11
DX12	DX Bus Bit 12
DX13	DX Bus Bit 13
DX14	DX Bus Bit 14
DX15	DX Bus Bit 15
FNB0	Function Bit 0
FNB1	Function Bit 1
FNB2	Function Bit 3
ICLKM	I-Board Clock - MOS
ICLKT	I-Board Clock - TTL
ICLKT-	I-Board Clock - TTL, Active Low
ID01	Identification Bit 1
ID02	Identification Bit 2
ID03	Identification Bit 3
IE	Interrupt Enable
IE0	Interrupt Enable Priority 0
IE1	Interrupt Enable Priority 1
IE2	Interrupt Enable Priority 2
IE3	Interrupt Enable Priority 3
IE4I	Interrupt Enable Level 4 Input
IE4O	Interrupt Enable Level 4 Output
IEO	Interrupt Enable Out
INTACK	Interrupt Acknowledge
LED0	Light Emitting Diode 0
LED1	Light Emitting Diode 1
LED2	Light Emitting Diode 2
LED3	Light Emitting Diode 3
LED4	Light Emitting Diode 4
LED5	Light Emitting Diode 5
LED6	Light Emitting Diode 6
LED7	Light Emitting Diode 7
LEDEN-	LED Enable
LEDSWEN-	LED/DIP Switch I/O Port Address
MAS0	Memory Address Select Phase 0
MAS1	Memory Address Select Phase 1
MAS2	Memory Address Select Phase 2
MCLKT	M-Board Clock, TTL
MDBC	Mode Bit C
MDBD	Mode Bit D
MDCA	Mode Control A
MDCB	Mode Control B
MEMWAIT	Memory Wait State
MREQ	Memory Request
PCLKM	P-Board Clock (MOS)
PCLKT	P-Board Clock (TTL)
PCQ1	Pre Charge Extender Q-Output 1
PCQ2-	Pre Charge Extender Q-Output 2
PS0	Processor Status Bit 0
PS1	Processor Status Bit 1
PS2	Processor Status Bit 2
PS3	Processor Status Bit 3
RADR00	ROM Address Bit 00

RADR01	ROM Address Bit 01
RADR02	ROM Address Bit 02
RADR02	ROM Address Bit 02
RADR03	ROM Address Bit 03
RADR04	ROM Address Bit 04
RADR05	ROM Address Bit 05
RADR06	ROM Address Bit 06
RADR07	ROM Address Bit 07
RADR08	ROM Address Bit 08
RADR09	ROM Address Bit 09
RADR10	ROM Address Bit 10
RADR11	ROM Address Bit 11
RADR12	ROM Address Bit 12
RADR13	ROM Address Bit 13
RADR14	ROM Address Bit 14
RAME	RAM Wait Enable
RAMEN	RAM Wait Enable
RAMOEN-	RAM Output Enable
RAS-	Row Address Select (Attenuated)
RASD-	Row Address Select (Unattenuated)
RC0-	Serial Receive Clock Channel 0
RC1-	Serial Receive Clock Channel 1
RACACK-	Receive Address Clock
RCAE-	Receive Address Output Enable
RCAS0	RAM Column Address Select 0
RCAS1	RAM Column Address Select 1
RCSCK	Receive Control and Status Register Clock
RCSE	Receive Control and Status Register Output Enable
RCSR03	Receive Control/Status Register Bit 03
RD	Read Transmit Data Buffer
RD0	Receive Data Channel 0
RD1	Receive Data Channel 1
RDAT0	ROM Data Bit 0
RDAT1	ROM Data Bit 1
RDAT2	ROM Data Bit 2
RDAT3	ROM Data Bit 3
RDAT4	ROM Data Bit 4
RDAT5	ROM Data Bit 5
RDAT6	ROM Data Bit 6
RDAT7	ROM Data Bit 7
RDBE	Receive Data Buffer Output Eanble
RDBG	Receive Data Buffer Flag
RDBFA	Read Data Buffer Full, Term A
RDQ-	Read Request
RDREG-	Read 4 X 4 Register File
RDZRCR	Read Z80 Receive Control Register
READFN-	MDMA Read Function
REM16	Receive Extended Memory Address Bit 16
REM17	Receive Extended Memory Address Bit 17
RESETA-	Reset Term A
RESETB-	Reset Term B
RESETC-	Reset Term C
RGO	Receive Go Bit
RIEN	Receive Interrupt Enable
RIRDY-	Receive Interrupt Ready
RIRDYG-	Receive Interrupt Ready Enabled

RLFULL	Receive Low Byte Full
RLFULLJ	Receive Low Byte Full, J Input
RMERR	Receive Memory Error
RNG0H	Ring Indicator Channel 0, + Term to Receiver
RNG0HI	Ring Indicator Channel 0, + Term on Input Connector
RNG0L	Ring Indicator Channel 0, - Term to Receiver
RNG1H	Ring Indicator Channel 1, + Term on Input Connector
RNG1HI	Ring Indicator Channel 1, + Term to Receiver
RNG1L	Ring Indicator Channel 1, - Term on Input Connector
ROM-	ROM Address Decode
ROME	ROM Wait Enable
ROMEN	ROM Wait Enable
ROMP23	ROM Pin 23
RRESET-	Receive Channel Reset
RSETSIG	Receive Set Signal
RSIGEN	Recieve Signal Enable
RSIGENS	Receive Signal Enable Synchronized
RSIGJ	Receive Signal, J Input
RSIGNAL	Receive Signal
RSIGSET	Receive Signal Set
RSTOP	Receive Channel Stop
RSTP	Receive Stop
RSVC-	Recieve Vector Decode
RTCA	Rise Time Control A
RTCB	Rise Time Control B
RTCC	Rise Time Control C
RTCD	Rise Time Control D
RTCE	Rise Time Control E
RTCF	Rise Time Control F
RTCG	Rise Time Control G
RTCH	Rise Time Control H
RTCI	Rise Time Control I
RTCJ	Rise Time Control J
RTCK	Rise Time Control K
RTCL	Rise Time Control L
RTCM	Rise Time Control M
RTCN	Rise Time Control N
RTCO	Rise Time Control O
RTCP	Rise Time Control P
RUFULL	Receive Upper Byte Full
RVSEL	Receive Vector Select
RWCCK-	Receive Word Count Register Clock
RWCE-	Receive Word Count Register Output Enable
RX-	Baud Rate Generator, Receive Clock
RXC0-	Receive Clock Channel 0
RXC0H	Receive Clock Channel 0, + Term to Reciever
RXC0HI	Receive Clock Channel 0, + Term on Input Connector
RXC0L	Receive Clock Channel 0, - Term to Receiver
RXC0LI	Receive Clock Channel 0, - Term on Input Connector
RXC1-	Receive Clock Channel 1
RXC1H	Receive Clock Channel 1, + Term to Receiver
RXC1HI	Receive Clock Channel 1, + Term on Input Connector
RXC1L	Receive Clock Channel 1, - Term to Receiver
RXC1LI	Receive Clock Channel 1, - Term on Input Connector
RXD0H	Receive Data Channel 0, + Term to Receiver
RXD0HI	Receive Data Channel 0, + Term on Input Connector

RXD0L	Receive Data Channel 0, - Term to Receiver
RXD0LI	Receive Data Channel 0, - Term on Input Connector
RXD1H	Receive Data Channel 1, + Term to Receiver
RXD1HI	Receive Data Channel 1, + Term on Input Connector
RXD1L	Receive Data Channel 1, - Term to Receiver
RXD1LI	Receive Data Channel 1, - Term on Input Connector
SEL	MDMA Device Select
SERIALEN-	Serial Port Enable
SERRD	Serial Port Read
SIOEN-	SIO Chip Enable
SIORDYA	SIO Ready Channel A
SIORDYB	SIO Ready Channel B
SVCR-	Send ID Vector
SW0-	Switch Bit 0
SW1-	Switch Bit 1
SW2-	Switch Bit 2
SW3-	Switch Bit 3
SW4-	Switch Bit 4
SW5-	Switch Bit 5
SW5-	Switch Bit 5
SW6-	Switch Bit 6
SW7-	Switch Bit 7
SWEN-	DIP Switch Enable
TCACK-	Transmit Address Clock
TCAE-	Transmit Address Output Enable
TCM0H	Transmit Clock from Modem Channel 0, + Term to Receiver
TCM0HI	Transmit Clock from Modem Channel 0, + Term on Input Connector
TCM0L	Transmit Clock from Modem Channel 0, - Term to Reciever
TCM0LI	Transmit Clock from Modem Channel 0, - Term on Input Connector
TCM1H	Transmit Clock from Modem Channel 1, + Term to Receiver
TCM1HL	Transmit Clock from Modem Channel 1, + Term on Input Connector
TCM1L	Transmit Clock from Modem Channel 1, - Term to Reciever
TCM1LI	Transmit Clock from Modem Channel 1, - Term on Input Connector
TCSCK	Transmit Control and Status Register Clock
TCSE-	Transmit Control and Status Register Output Enable
TSCR09	Transmit Control and Status Register Bit 09
TCT0H	Transmit Clock from Terminal Channel 0, + Term from Driver
TCT0HO	Transmit Clock from Terminal Channel 0, + Term on Output Connector
TCT0L	Transmit Clock from Terminal Channel 0, - Term from Driver
TCT0LO	Transmit Clock from Terminal Channel 0, - Term on Output Connector
TCT1H	Transmit Clock from Terminal Channel 1, + Term from Driver
TCT1HO	Transmit Clock from Terminal Channel 1, + Term on Output Connector
TCT1L	Transmit Clock from Terminal Channel 1, - Term from Driver
TCT1LO	Transmit Clock from Terminal Channel 1, - Term on Output Connector
TD0	Transmit Data Channel 0
TD1	Transmit Data Channel 1
TDAT0	Transmit Data Buffer Bit 0
TDAT1	Transmit Data Buffer Bit 1

TDAT2	Transmit Data Buffer Bit 2
TDAT3	Transmit Data Buffer Bit 3
TDAT4	Transmit Data Buffer Bit 4
TDAT5	Transmit Data Buffer Bit 5
TDAT6	Transmit Data Buffer Bit 6
TDAT7	Transmit Data Buffer Bit 7
TDBCK	Transmit Data Buffer Clock
TDBFULL	Transmit Data Buffer Full
TDBL	Transmit Data Buffer Low Byte
TDBLOE	Transmit Data Buffer Low Byte Output Enable
TDBU	Transmit Data Buffer Upper Byte
TDBUOE	Transmit Data Buffer Upper Byte Output Enable
TEM16	Transmit Extended Memroy Address Bit 16
TEM17	Transmit Extended Memroy Address Bit 17
TGO	Transmit Channel Go Bit
TIEN	Transmit Interrupt Enable
TIRDY-	Transmit Interrupt Ready
TIRDYG-	Transmit Interrupt Ready Enable
TM0-	Transmit Clock from Modem Channel 0
TM1-	Transmit Clock from Modem Channel 1
TMERR	Transmit Memory Error
TODD	Transmit Odd Number of Bytes
TRESET-	Transmit Channel Reset
TSETA	Transmit Signal Set Term A
TSIGJ	Transmit Signal J Term
TSIGNAL	Transmit Signal
TSTOP	Transmit DMA Stop
TSVC-	Transmit Send Vector
TT0-	Terminal Timing Channel 0
TT1-	Terminal Timing Channel 1
TVSEL	Transmit Vector Select
TWCCK-	Transmit Word Count Register Clock
TWCE-	Transmit Word Count Register Output Enable
TX-	Baud Rate Generator, Transmit Clock
TXC0-	Transmit clock Channel 0
TXC1-	Transmit Clock Channel 1
TXD0H	Transmit Data Channel 0, + Term from Driver
TXD0HO	Transmit Data Channel 0,
TXD0L	Transmit Data Channel 0,
TXD0LO	Transmit Data Channel 0,
TXD1H	Transmit Data Channel 1,
TXD1HO	Transmit Data Channel 1,
TXD1L	Transmit Data Channel 1,
TXD1LO	Transmit Data Channel 0,
VCT03	Interrupt Vector Bit 3
VCT04	Interrupt Vector Bit 4
VCT05	Interrupt Vector Bit 5
VCT06	Interrupt Vector Bit 6
VCT07	Interrupt Vector Bit 7
VECTFN-	MDMA Vector Function
VECTR-	Vector
VM	Voltage Pullup on M-Board
VP	Voltage Pullup on P-Board
W-	Write
WAITEN	Memory M1 Cycle Wait Enable
WAITRES-	Wait Reset

WRREG-	Write into 4 X 4 Register Files
WRT-	Write
WRTFN-	MDMA Write Function
XBAD00	X-Bus Address Bit 00
XBAD01	X-Bus Address Bit 01
XBAD02	X-Bus Address Bit 02
XBAD03	X-Bus Address Bit 03
XBAD04	X-Bus Address Bit 04
XBAD05	X-Bus Address Bit 05
XBAD06	X-Bus Address Bit 06
XBAD07	X-Bus Address Bit 07
XBCLK	X-Bus Clock (Active Falling Edge)
XBCNT0	X-Bus Control Bit 0
XBCNT1	X-Bus Control Bit 1
XBCNT2	X-Bus Control Bit 2
XBDA00	X-Bus Data Bit 00
XBDA01	X-Bus Data Bit 01
XBDA02	X-Bus Data Bit 02
XBDA03	X-Bus Data Bit 03
XBDA04	X-Bus Data Bit 04
XBDA05	X-Bus Data Bit 05
XBDA06	X-Bus Data Bit 06
XBDA07	X-Bus Data Bit 07
XBDA08	X-Bus Data Bit 08
XBDA09	X-Bus Data Bit 09
XBDA10	X-Bus Data Bit 10
XBDA11	X-Bus Data Bit 11
XBDA12	X-Bus Data Bit 12
XBDA13	X-Bus Data Bit 13
XBDA14	X-Bus Data Bit 14
XBDA15	X-Bus Data Bit 15
XBEOT	X-Bus End of Transfer
XBRDY-	X-Bus Ready Bit
XBRST	X-Bus Reset
ZADR00	Z80 Address Bit 00
ZADR01	Z80 Address Bit 01
ZADR02	Z80 Address Bit 02
ZADR03	Z80 Address Bit 03
ZADR04	Z80 Address Bit 04
ZADR05	Z80 Address Bit 05
ZADR06	Z80 Address Bit 06
ZADR07	Z80 Address Bit 07
ZADR08	Z80 Address Bit 08
ZADR09	Z80 Address Bit 09
ZADR10	Z80 Address Bit 10
ZADR11	Z80 Address Bit 11
ZADR12	Z80 Address Bit 12
ZADR13	Z80 Address Bit 13
ZADR14	Z80 Address Bit 14
ZADR15	Z80 Address Bit 15
ZBUSRZ-	Z80 Bus Request
ZDAT0	Z80 Data Bit 0
ZDAT1	Z80 Data Bit 1
ZDAT2	Z80 Data Bit 2
ZDAT3	Z80 Data Bit 3
ZDAT4	Z80 Data Bit 4

ZDAT5	Z80 Data Bit 5
ZDAT6	Z80 Data Bit 6
ZDAT7	Z80 Data Bit 7
ZDBOE	Z80 Data Buffer Output Enable
ZDBOES	Z80 Data Buffer Output Enable Synchronize
ZHALT-	Z80 Halt State
ZINT-	Z80 Interrupt Request
ZIORQ-	Z80 Input/Output Request
ZM1	Z80 Machine Cycle One
ZMREQ-	Z80 Memory Request
ZRCREN-	Z80 Receiver Control Register Enable
ZRCROE-	Z80 Receive Control Register Output Enable
ZRCYL	Z80 Receive Cycle
ZRD-	Z80 Memory Read
ZRDATEN-	Z80 Receive Data Register Eanble
ZRES-	Z80 Reset
ZRES1	Z80 Reset Term 1
ZRESQ-	Z80 Reset Q Output
ZRFSH	Z80 Refresh
ZS0	Z80 Status Bit 0
ZS1	Z80 Status Bit 1
ZS2	Z80 Status Bit 2
ZS3	Z80 Status Bit 3
ZTCRCLK	Z80 Transmit Control Register Clock
ZTCREN	Z80 Transmit Control Register Enable
ZTCROE-	Z80 Transmit Control Register Output Enable
ZTCYL	Z80 Transmit Cycle
ZTDATEN-	Z80 Transmit Data Register Enable
ZTDATWR	Z80 Transmit Data Register Write
ZTDATWRS	Z80 Transmit Data Register Write Synchronized
ZTFULL	Z80 Transmit Data Buffer Full
ZTFULLK	Z80 Transmit Data Buffer Full K Input
ZWAIT-	Z80 Wait
ZWR	Z80 Memory Write

* SIGNAL NAME GLOSSARY - DRAWING 2600429

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